Amendments to the Specification:

Please amend page 14 by deleting the title and inventor name.

Also, please amend the body of the abstract as follows. A clean copy of the following abstract is included on a separate sheet, after the Remarks section.

A packet crosspoint ~~that cross-connects asynchronous UBR (unspecified bit rate) packet traffic received at n inputs to any of n outputs is disclosed that buffers the packets at both the n input ports as well as the n output ports. The crosspoint~~ works with an arbiter to control the number of packets being received at the input ports of the cross-connect from traffic sources coupled thereto. This is accomplished by monitoring the number of packets waiting in buffers in the output ports, as well as the number of other packets which the arbiter has already granted for transmission to the input ports of the cross-connect, but which have not as of yet been received in the output queue of the destination output port. ~~This mechanism serves to keep the input port buffer from backing up to avoid "head-of-line" blocking problems. The number of grants issued by an arbiter can also be throttled based on back-pressure signals provided by the input buffers in the even that they start to back up to avoid losing packets when input buffers overflow.~~ An audit mechanism is included for ensuring that output port grant counters do not drift upward based on the fact that some granted packets are lost in the system. ~~Finally, back-pressure may also be asserted by the destination for traffic output from the cross-connect to slow down the output of cross-connected traffic in the event that they are issued faster than the traffic receiver can process them.~~

Please amend a paragraph at page 2 lines 6-18 as follows.

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Until recently, service providers have had to maintain separate network fabrics (or overlays) to handle these various classes of traffic. Maintaining separate overlays is expensive and makes network management very complex. As a result, application of

mixed class access systems to the lower end of the network is too costly. Thus, it would be highly desirable to provide a single network access system that is capable of flexibly handling a broad mix of traffic classes, including both synchronous and asynchronous traffic types. Further, it would be desirable for this system to be capable of flexible configuration to perform multiple network functions such as network access system, a digital loop carrier (DLC), a transport level add/drop mux, etc. Such a system would require as one of its components an asynchronous packet cross-connect to route the asynchronous traffic such as UBR (unspecified bit rate) in the form of ATM unicast traffic. Those of skill in the art will recognize that an access system capable of handling a broad mix of traffic classes will require novel and non-obvious methods and apparatuses.

Please amend a paragraph at page 2 line 20 to page 3 line 7 as follows.

~~The~~ An asynchronous cross-connect ~~of the present~~ in accordance with the invention switches asynchronous packet data, received from one or more traffic sources, between ~~a plurality of I/O~~ input and output ports. Both the input and output ports are buffered. The outputs are buffered in the event that once cross- connected, the packets may have to wait before they can be read from the output port by their respective data sinks. The number of packets permitted to be released ~~to receive and store packets~~ are stored until they can be transmitted between their input and destination ports, and further until the data is released from the output port to its destination in a network. The number of packets being sent to the inputs of the cross-connect is controlled by the number of grants issued by an ~~arbitration unit~~ arbiter to the traffic sources. The rate of grants is controlled by several signals. First, there is a threshold on the number of packets allowed in the output buffers. If the number is exceeded, a signal is issued to cease grants for the output having the full buffer. Additionally, ~~the arbiter~~ a grant counter associated with each output keeps track of all packets in the system for ~~each~~ that output, and if the total number of packets in the system exceeds some threshold, the arbiter ceases granting any packets until the number of packets in the system destined for a particular output falls below some number.

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The output buffers are regulated first to avoid affecting the inputs and risking head-of-line blocking. ~~Additionally, the input buffers also provide a backpressure signal when their threshold is exceeded.~~ Finally a grant audit is conducted periodically to prevent upward drift in grant counters on the outputs due to the loss of packets not received by the output buffers.

Please amend a paragraph at page 4 line 26 to page 5 line 10 as follows.

The arbiter 12 determines when packets are granted based on the VOQ images (queue occupancy) it maintains and the bandwidth allocation that has been provisioned for each of the source line cards 16a. Depending upon the type of line unit, an access processor (GAP) 22 or a routing and switch processor (RSP) 24 appends flow identification, routing information, and other overhead control fields to the incoming packets 26. A packet is transferred to the packet cross-connect 10 in a 64 byte format. The 64 byte fixed length packet (FLP) may be either an extended ATM cell or a data packet. The packet is connected via the packet cross-connect 10 to a destination output 19a-n based on the routing map included in the header of the packet. At the output, depending on the type of line unit 16b, the GAP 22 or the RSP 24 strips the appended flow identification and routing map information and transmits out from the system through physical interface circuit (PHY) 28. For detailed information regarding an embodiment of a system such as the one just disclosed, refer to related and co-filed U.S. Application ~~Attorney Docket No. M-11699 US~~ <u>09/874,352</u> entitled "Concurrent Switching of Synchronous and Asynchronous Traffic" by Jason Dove et al., and which is incorporated herein in its entirety, including all Figures and Attachments, by this reference

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Please amend a paragraph at page 8 lines 7-12 as follows.

~~Thee~~ <u>The</u> output port controller I22a-n performs the following functions. It arbitrates among multiple input ports 88a-n requesting a transfer of a packet to the associated output

FIFO 101a-n. Each output port controller's arbiter (150a-n, Fig. 5) examines the routing map assembled from the input FIFOs 100a-n and performs a round-robin arbitration. After determining a winner, the arbiter (150a-n, Fig. 5) performs the control operations that transfer the packet from input to output.

Please amend a paragraph at page 11 line 26 to page 12 line 5 as follows.

[[5.]] When the "Terminate Grant Audit" type VOQ arrival message is received by the packet cross-connect 10, it translates the strobe/VOQ data to the appropriate strobe/grant counter identifier and enters the information in a queue that operates in parallel with the associated input FIFO. The audit terminate flag emerges from the queue and is passed to the output port as the packet it arrived with is transferred across the cross-connect. When the output port controller receives the terminate flag, the decrement of the saved grant counter is stopped after counting the associated packet. Any remainder in the counter indicates the amount of error. The remainder is automatically applied to the grant counter under audit to correct the error. The termination and amount of error are reported to management software. This prevents any of the grant counters from drifting upwards due to lost packets granted but not processed.

Please amend a paragraph at page 12 lines 6-16 as follows.

Those of skill in the art will recognize that the packet cross-connect of the present invention is not tied to the system in which such a cross-connect can reside. The system context provided herein is exemplary only, and is used to convey the manner in which the cross-connect of the present invention would interact with such a system. Provided that similar interface signals are provided between the cross-connect of the present invention and the system context in which it is employed, the present invention, as well as the features thereof, remains patentably distinct from the system. For more information regarding the interface and implementation details of the present invention, please refer to

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the GRX ASIC Packet Crosspoint Module Specification, attached as Attachment C to related and co-filed U.S. Application ~~Attorney Docket No. M-11699 US~~ 09/874,352 entitled "Concurrent Switching of Synchronous and Asynchronous Traffic" by Jason Dove et al.

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